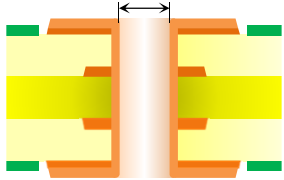
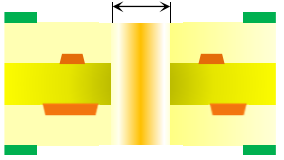




## Technical Capabilities for Multilayer PCB's

Item	Minimum Capability	Maximum Capability	Tolerance	Remarks
<b>Metal Finishing:</b> Hal Lead Free (SnCuNi) Chemical Tin (Inm.Sn) (*) Chemical Silver (Inm.Ag) Electroless Ni Immersion Gold (ENIG)	Ni: 3 µm Au: 0,04 µm	Ni: 7 µm Au: 0,07 µm	-	Sn100C Alloyage (*) Subcontracted
<b>Final Finishing:</b> Liquid PhotoImageable Solder Mask Ink Legend Conductive Carbon Ink Peelable Mask	-	-	-	A wide range of colours A wide range of colours
<b>Raw Material:</b> FR-4 Tg Standard FR-4 High Tg	130 °C 150 °C	140°C 180 °C	-	Depending on the manufacturer
<b>Number of layers</b>	4	8	-	Under request (consult delivery time): 105 µm
<b>Base Copper (inner or outer layers)</b>	17 µm	70 µm	-	Or equivalent tolerance
<b>Plated Through Hole (PTH)</b> 	200 µm	-	+ 0,10 / - 0,05 mm	Or equivalent tolerance
<b>Non Plated Through Hole (NPTH)</b> 	300 µm	-	+ 0,10 / - 0 mm	O tolerancia equivalente



## Technical Capabilities for Multilayer PCB's

Item	Minimum Capability	Maximum Capability	Tolerance	Remarks
Width and isolation of copper conductors in outer layers (Base Copper)	 100 µm (17 µm)		± 25%	
	 125 µm (35 µm)	-	± 30%	
	 200 µm (70 µm)		± 30%	
Width and isolation of copper conductors in inner layers (Base Copper)	 100 µm (17 µm)		± 25%	
	 100 µm (35 µm)	-	± 25%	
	 200 µm (70 µm)		± 30%	
Copper annular ring in outer layers (Base Copper)	 100 µm (17 µm)			Recommendation: for a good soldering surface, for component holes ≥ 200 µm
	 125 µm (35 µm)	-	-	
	 250 µm (70 µm)			
Copper annular ring in inner layers (Base Copper)	 150 µm	-	-	
Minimal isolation in inner layers (power and ground planes)	 250 µm	-	-	
Distance between NPTH and copper conductor	 200 µm	-	-	

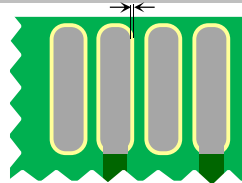
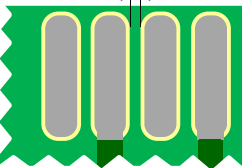
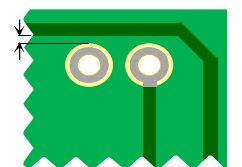
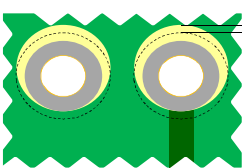
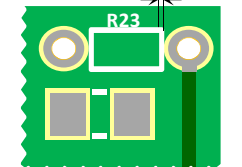
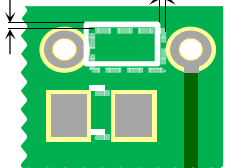


## Technical Capabilities for Multilayer PCB's

Item		Minimum Capability	Maximum Capability	Tolerance	Remarks
Distance between copper conductor and board edge (routed)		150 µm	-	-	-
Misalignment between copper and PTH		-	-	± 100 µm	-
Misalignment between outline and PTH		-	-	± 150 µm	-
Distance between a copper conductor and theoretical scoring axis		500 µm	-	-	-
Maximum hole to be plugged with peelable mask		0,30 mm	1,80 mm	-	-
Distance between peelable mask and copper pad		0,80 mm	-	-	-



## Technical Capabilities for Multilayer PCB's

Item	Minimum Capability	Maximum Capability	Tolerance	Remarks
Solder Mask annular ring 	50 $\mu\text{m}$	-	-	-
Solder Mask bridge 	100 $\mu\text{m}$	-	-	-
Distance between solder mask clearance and copper conductor 	50 $\mu\text{m}$	-	-	-
Misalignment between solder mask and copper 	-	-	$\pm 150 \mu\text{m}$	-
Ink Legend width 	100 $\mu\text{m}$	-	-	-
Misalignment between ink legend and copper 	-	-	$\pm 200 \mu\text{m}$	-

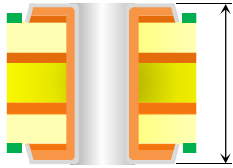
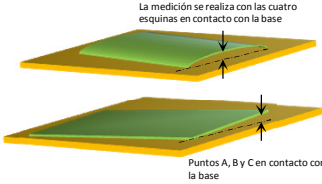
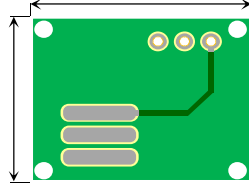


## Technical Capabilities for Multilayer PCB's

Item	Minimum Capability	Maximum Capability	Tolerance	Remarks
Carbon ink width	600 $\mu\text{m}$	-	-	-
Separation between carbon conductors	400 $\mu\text{m}$	-	-	-
Platted Wall thickness	20 $\mu\text{m}$	60 $\mu\text{m}$	-	Average: 25 $\mu\text{m}$
Scoring positioning (taken on axis)	-	-	$\pm 150 \mu\text{m}$	-
Core thickness after scoring process	200 $\mu\text{m}$	-	$\pm 150 \mu\text{m}$	Standard: 300 $\mu\text{m}$
Misalignment between top-bottom scoring blades	-	-	$\pm 150 \mu\text{m}$	-



## Technical Capabilities for Multilayer PCB's

Item	Minimum Capability	Maximum Capability	Tolerance	Remarks
<b>Final Thickness</b> 	0,80 mm	3,2 mm	$\pm 10\%$ ( $e > 1,0$ mm) $\pm 100\ \mu\text{m}$ ( $e \leq 1,0$ mm)	Depending on Multilayer stack-up and number of layers
<b>Bow &amp; Twist</b> 	-	0,75% of diagonal	-	-
<b>Final pcb dimensions (routing)</b> 	15 x 15 mm	510 x 370 mm	$< 30$ mm: $\pm 0.10$ mm $< 120$ mm: $\pm 0.15$ mm $> 120$ mm: $\pm 0.20$ mm	-
<b>Other</b>	-	-	-	According to IPC-A-600 revision G Standard

### REMARKS

- 1.- The extra Cu deposition is performed by an electrolytic process; therefore It is extremely convenient that the density of Cu on both sides is similar. This reduces the irregularities in total Cu thickness, warping and bending, reduction in PTH diameters and the excess of Cu on conductors.
- 2.- It is important to eliminate nonfunctional pads on the inner layers (usually placed where PHTs go with no connection on that particular layer) in order to avoid short circuits
- 3.- For class VI and VII PCBs the use of tear drops is highly recommended to compensate the quantity of Cu on both sides