ZVBELZV S.L.

CIRCUITOS IMPRESOS - PRINTED CIRCUIT BOARDS

Technical Capabilities for Multilayer PCB´s

Item	Minimum Capability	Maximum Capability	Tolerance	Remarks
Metal Finishing:				
Hal Lead Free (SnCuNi)			-	Sn100C Alloyage
Chemical Tin (Inm.Sn) (*)				(*) Subcontracted
Chemical Silver (Inm.Ag)				
Electroless Ni Inmersion Gold (ENIG)	Ni: 3 µm Au: 0,04 µm	Ni: 7 µm Au: 0,07 µm		
Final Finishing:				
Liquid PhotoImageable Solder Mask	-	-	-	A wide range of colours
Ink Legend				A wide range of colours
Conductive Carbon Ink				
Peelable Mask				
Raw Material:				
FR-4 Tg Standard	130 ºC	140ºC	-	Depending on the manufacturer
FR-4 High Tg	150 ºC	180 ºC		
Number of layers	4	8	-	Under request (consult delivery time): 105 µm
Base Copper (inner or outter layers)	17 µm	70 µm	-	Or equivalent tolerance
Plated Through Hole (PTH)	200 µm	-	+ 0,10 / - 0,05 mm	Or equivalent tolerance
Non Plated Through Hole (NPTH)	300 µm	-	+ 0,10 / -0 mm	O tolerancia equivalente

ZVBELZV S.L.

CIRCUITOS IMPRESOS - PRINTED CIRCUIT BOARDS

Technical Capabilities for Multilayer PCB´s

Item	Minimum Capability	Maximum Capability	Tolerance	Remarks
Width and isolation of copper conductors in outter layers (Base Copper)	100 µm (17 µm) 125 µm (35 µm) 200 µm (70 µm)	-	± 25% ± 30% ± 30%	-
Width and isolation of copper conductors in inner layers (Base Copper)	100 µm (17 µm) 100 µm (35 µm) 200 µm (70 µm)	-	± 25% ± 25% ± 30%	-
Copper annular ring in outter layers (Base Copper)	100 µm (17 µm) 125 µm (35 µm) 250 µm (70 µm)	-	-	Recommendation: for a good soldering surface, for component holes ≥ 200 µm
Copper annular ring in inner layers (Base Copper)	150 µm	-	-	-
Minimal isolation in inner layers (power and ground planes)	250 µm	-	-	-
Distance between NPTH and copper conductor	200 µm	-	-	-

ZVBELZV S.L.
CIRCUITOS IMPRESOS - PRINTED CIRCUIT BOARDS

Technical Capabilities for Multilayer PCB´s

Item	Minimum Capability	Maximum Capability	Tolerance	Remarks
Distance between copper conductor and board edge (routed)	150 µm	-	-	-
Misalignement between copper and PTH	-	-	± 100 µm	-
Misalignement between outline and PTH	-	-	± 150 µm	
Distance between a copper conductor and theorical scoring axis	500 µm	-	-	-
Maximum hole to be plugged with peelable mask	0,30 mm	1,80 mm	-	-
Distance between peelable mask and copper pad	0,80 mm	-	-	-

Technical Capabilities for Multilayer PCB´s

Item	Minimum Capability	Maximum Capability	Tolerance	Remarks
Solder Mask annular ring	50 µm	-	-	-
Solder Mask bridge	100 µm	-	-	-
Distance between solder mask clearance and copper conductor	50 µm	-	-	-
Misalignement between solder mask and copper	-	-	± 150 µm	-
Ink Legend width	100 µm	-	-	-
Misalignement between ink legend and copper	-	-	± 200 µm	-

ZVBELZV S.L.

CIRCUITOS IMPRESOS - PRINTED CIRCUIT BOARDS

Technical Capabilities for Multilayer PCB´s

Item	Minimum Capability	Maximum Capability	Tolerance	Remarks
Carbon ink width	600 µm	-	-	-
Separation between carbon conductors	400 µm	-	-	-
Platted Wall thickness	20 µm	60 µm	-	Average: 25 µm
Scoring positioning (taken on axis)	-	-	± 150 µm	-
Core thickness after scoring process	200 µm	-	± 150 µm	Standard: 300 µm
Misalignement between top-bottom scoring blades	-	-	± 150 µm	-

Technical Capabilities for Multilayer PCB´s

Item	Minimum Capability	Maximum Capability	Tolerance	Remarks
Final Thickness	0,80 mm	3,2 mm	± 10 % (e > 1,0 mm) ± 100 µm (e ≤ 1,0 mm)	Depending on Multilayer stack-up and number of layers
Bow & Twist La medición se realiza con las cuatro esquinas en contacto con la base Puntos A, B y C en contacto con la base	-	0,75% of diagonal	-	-
Final pcb dimensions (routing)	15 x 15 mm	510 x 370 mm	< 30 mm: ± 0.10 mm < 120 mm: ± 0.15 mm >120 mm: ± 0.20 mm	-
Other	-	-	-	According to IPC-A-600 revision G Standard

REMARKS

1.- The extra Cu deposition is performed by an electrolytic process; therefore It is extremely convenient that the density of Cu on both sides is similar. This reduces the irregularities in total Cu thickness, warping and bending, reduction in PTH diameters and the excess of Cu on conductors.

2.- It is important to eliminate nonfunctional pads on the inner layers (usually placed where PHTs go with no connection on that particular layer) in order to avoid short circuits

3.- For class VI and VII PCBs the use of tear drops is highly recommended to compensate the quantity of Cu on both sides